* **Register Description**

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| Register Name | Offset Address | Description |
| Control signals | 0x00 | Control signals Definition  bit 0 - ap\_start (Read/Write/COH)  Set 1 to start Axis DMA function  bit 1 - ap\_done (Read/COR)  bit 2 - ap\_idle (Read)  bit 3 - ap\_ready (Read/COR) |
| Buffer transfer done status register | 0x10 | bit 0 – buffer transfer done status (Read)  Set this register to 1 if stream data has written to memory and data length is equal to Buffer Length(1024 DW) |
| Buffer transfer done status clear register | 0x20 | bit 0 – clear buffer transfer done status (Read/Write)  Set 1 to clear buffer done status and reset internal state, then set 0 if finish to clear buffer done status  Note: After buffer transfer done status is clear, this register needs to be cleared for next operation. |
| Buffer Length | 0x28 | Set buffer length, must set to 1024. |
| Triggered condition | 0x30 | bit 23~0 –Set the Triggered condition (Read/Write)  Note: When the stream data [23:0] matches the triggered condition, the LA DMA engine will start putting data into the buffer in the memory until the data fills the buffer. |
| Buffer Lower base address register | 0x38 | bit 31~0 – The memory base address [31:0] of buffer (Read/Write) |
| Buffer Upper base address register | 0x3C | bit 31~0 – The memory base address [63:32] of buffer (Read/Write) |

* **Porting Guide**

1. Setup process
   1. Set Rx20 to 0x00, exit clear operation
   2. Set Rx28 to 1024, Set buffer length
   3. Set Rx30 for the triggered condition, only bit23~0 is valid
   4. Set Rx38, Rx3C for the memory base address of buffer
   5. Set Rx00[0] to 1, set ap\_start register to start the trigger operation
2. Data process
   1. Wait Rx10[0] == 1, indicate that stream data is matched with the triggered condition and the received data fills full the buffer from this triggered point
   2. Read all data from buffer
3. Status clear process
   1. Set Rx20[0] to 1, clear Buffer transfer done status clear register and reset internal state
   2. Set Rx00[0] to 1, set ap\_start register to start the trigger operation
   3. Wait Rx10[0] == 0, confirm status is cleared
   4. Set Rx20[0] to 0, exit clear operation for the next trigger operation